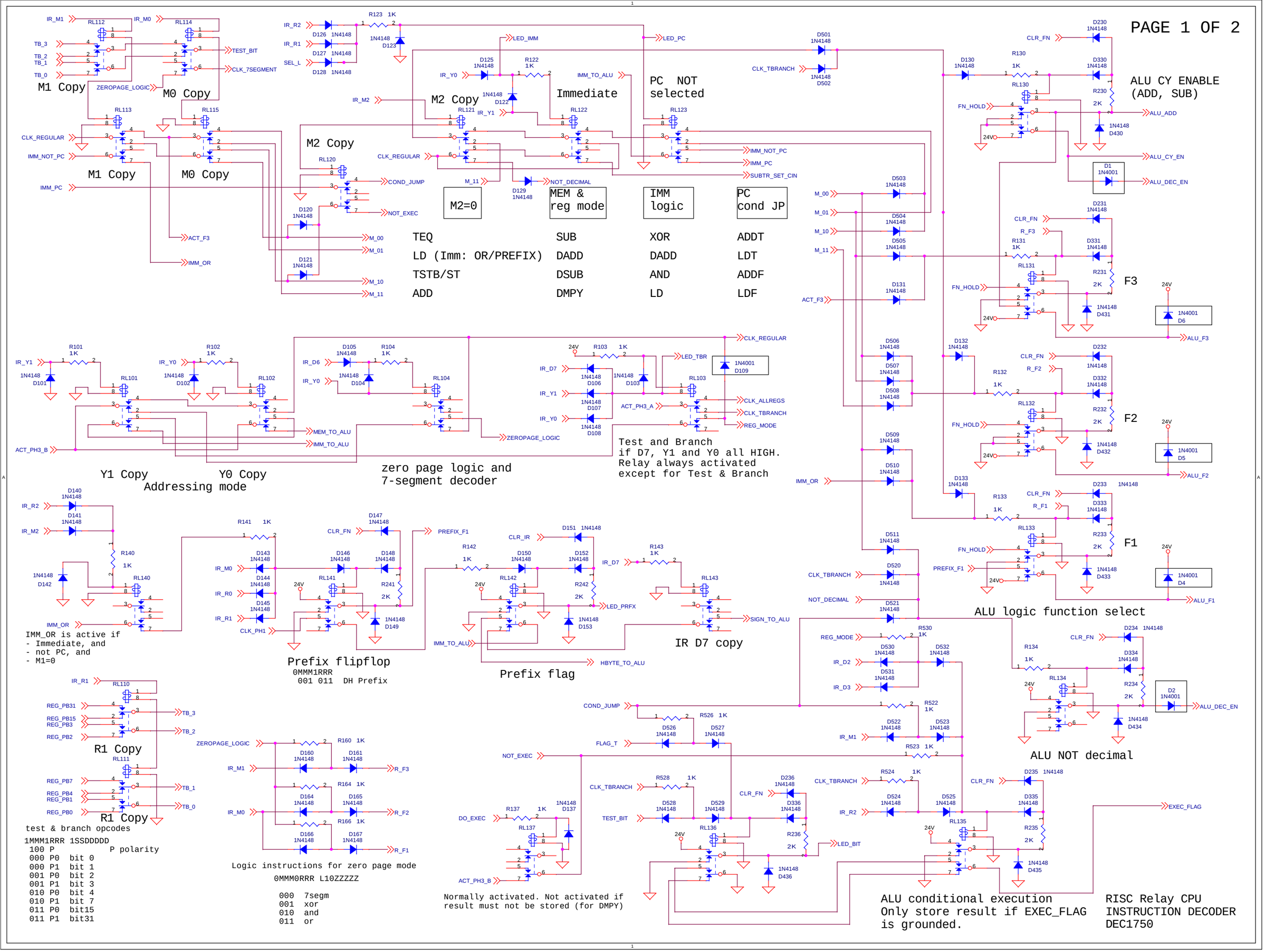
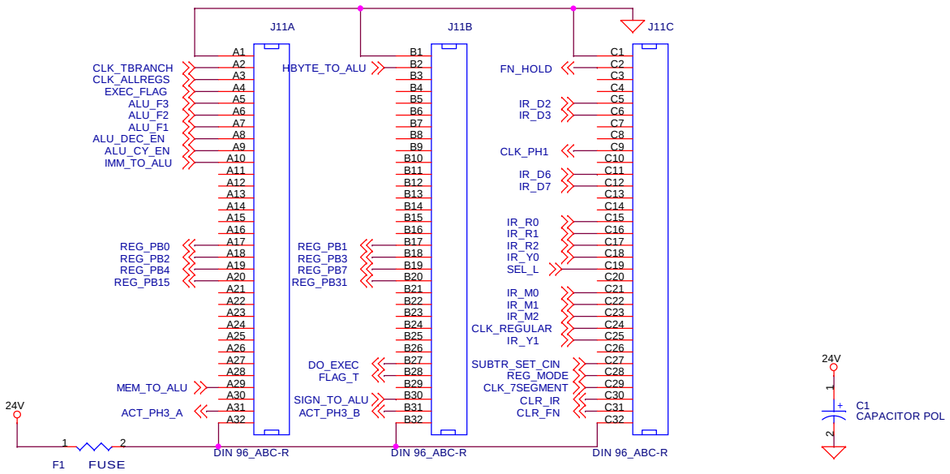
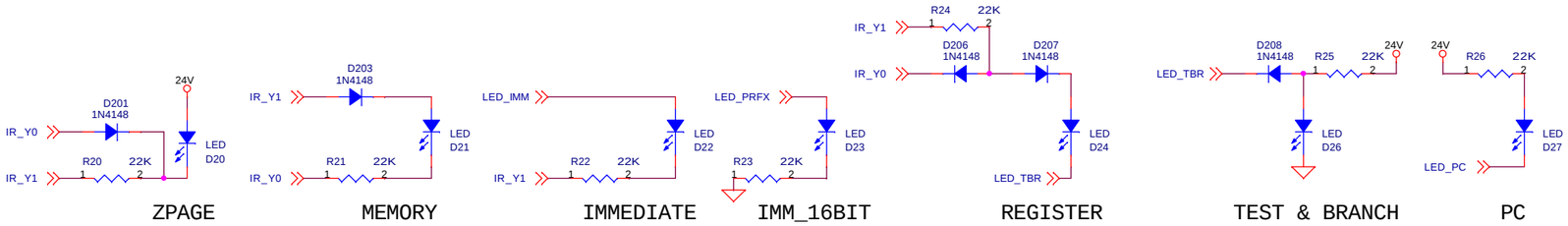
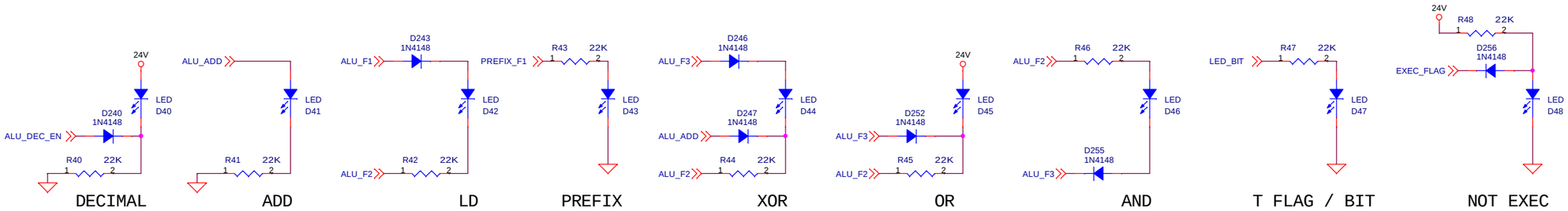

PAGE 1 OF 2
M1 Copy
M0 Copy
M2 Copy
Immediate
PC NOT selected
ALU CY ENABLE (ADD, SUB)
M2=0
MEM & reg mode
IMM logic
PC cond JP
TEQ
LD (Imm: OR/PREFIX)
TSTB/ST
ADD
SUB
DADD
DSUB
DMPY
XOR
DADD
AND
LD
ADDT
LDT
ADDF
LDF
F3
F2
F1
Y1 Copy
Y0 Copy
Addressing mode
zero page logic and
7-segment decoder
Test and Branch
if D7, Y1 and Y0 all HIGH.
Relay always activated
except for Test & Branch
IMM_OR is active if
- Immediate, and
- not PC, and
- M1=0
Prefix flipflop
0MMM1RRR
001 011 DH Prefix
Prefix flag
IR D7 copy
ALU logic function select
ALU NOT decimal
R1 Copy
R1 Copy
test & branch opcodes
1MMM1RRR 1SSDDDDD
100 P P polarity
000 P0 bit 0
000 P1 bit 1
001 P0 bit 2
001 P1 bit 3
010 P0 bit 4
010 P1 bit 7
011 P0 bit15
011 P1 bit31
Logic instructions for zero page mode
0MMM0RRR L10ZZZZZ
000 7segm
001 xor
010 and
011 or
Normally activated. Not activated if
result must not be stored (for DMPY)
ALU conditional execution
Only store result if EXEC_FLAG
is grounded.
RISC Relay CPU
INSTRUCTION DECODER
DEC1750







RISC Relay CPU
INSTRUCTION DECODER
DEC1750